In the Claims:

1. (Currently amended) A line card circuit comprising:

an activity latch for holding an activity flag value, wherein the activity flag value is mutually exclusive with a second activity flag value held in a second activity latch of a second line card circuit; and

a logic element operatively coupled to the activity latch to receive an incoming clock signal and to provide an outgoing clock signal, the outgoing clock signal being dependent on the activity flag value.

2. (Canceled)

3. (Original) The line card circuit of claim 1 wherein the logic element passes the incoming clock signal as the outgoing clock signal when the activity flag value has a first value.

4. (Original) The line card circuit of claim 3 wherein the logic element blocks the incoming clock signal when the activity flag value has a second value.

5. (Original) The line card circuit of claim 4 wherein the logic element provides a static output level as the output clock signal when the activity flag value has the second value.

6. (Withdrawn) A control card circuit comprising:

a redundancy configuration register for storing redundancy configuration flag values;

a first clock input;

a second clock input;

a logic circuit coupled to the redundancy configuration register, the first clock input, and the second clock input, the logic circuit automatically selecting a clock signal from among the first clock input and the second clock input when the redundancy configuration flag value has a first value.

7. (Withdrawn) The control card circuit of claim 6 wherein the logic circuit passes the first clock input and the second clock input when the redundancy configuration flag value has a second value.

8. (Withdrawn) The control card circuit of claim 7 further comprising:

a multiplexer operatively coupled to the logic circuit for receiving the clock signal when the redundancy configuration flag value has a first value.

9. (Withdrawn) The control card circuit of claim 8 wherein the multiplexer receives the first clock input and the second clock input when the redundancy configuration flag value has the second value.

10. (Withdrawn) The control card circuit of claim 9 wherein the logic circuit comprises combinational logic.

11. (Original) A method for selecting a syncronization source among a plurality of line card circuits comprising the steps of:

receiving a first activity flag value from a first activity latch of a first line card circuit of the plurality of line card circuits;

receiving an incoming clock signal;

providing an outgoing clock signal as the synchronization source dependent on the first activity flag value.

12. (Original) The method of claim 11 further comprising the step of:

receiving a second activity flag value from a second activity latch of a second line card circuit of the plurality of line card circuits, the second activity flag value being mutually exclusive of the first activity flag value.

13. (Original) The method of claim 11 wherein the step of providing the outgoing clock signal as the synchronization source dependent on the first activity flag value further comprises the step of:

passing the incoming clock signal as the outgoing clock signal when the first activity flag value has a passing value.

14. (Original) The method of claim 11 wherein the step of providing the outgoing clock signal as the synchronization source dependent on the first activity flag value further comprises the step of:

blocking the incoming clock signal when the first activity flag value has a blocking value.

15. (Original) The method of claim 14 wherein the step of providing the outgoing clock signal as the synchronization source dependent on the first activity flag value further comprises the step of:

providing a static output level as the outgoing clock signal when the first activity flag value has a blocking value.

16. (Withdrawn) A method for selecting a syncronization source among a plurality of line card circuits comprising the steps of:

receiving a first clock input from a first line card circuit of the plurality of line card circuits;

receiving a second clock input from a second line card circuit of the plurality of line card circuits;

when a redundancy configuration flag value has a first value, automatically selecting a clock signal as the synchronization source from among the first clock input and the second clock input.

17. (Withdrawn) The method of claim 16 further comprising the step of:

when a redundancy configuration flag value has a second value, passing the first clock input and the second clock input.

18. (Withdrawn) The method of claim 17 further comprising the step of:

when the redundancy configuration flag value has the first value, receiving the clock signal at a multiplexer.

19. (Withdrawn) The method of claim 18 further comprising the step of:

when the redundancy configuration flag value has the second value, receiving the first clock input and the second clock input at the multiplexer.